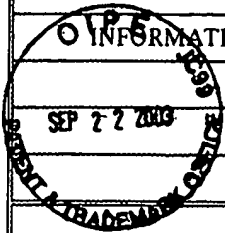





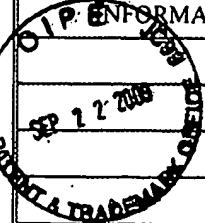
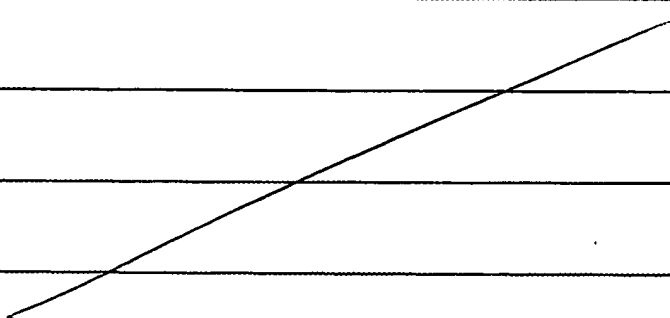


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				M-15222 US		10/632,155	
 INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary)				Applicant			
				Yi Ding			
				Filing Date		Group	
				July 30, 2003		Unassigned	
U.S. Patent Documents							
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	AA						
	AB						
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	AN						
	AO						
	AP						
	AQ						
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)							
	AR	United States Patent Application No. 10/440,466, entitled "Fabrication Of Conductive Gates For Nonvolatile Memories From Layers With Protruding Portions," Filed on May 16, 2003; Attorney Docket No.: M-12979 US.					
	AS	United States Patent Application No. 10/440,005, entitled "Fabrication of Dielectric On A Gate Surface To Insulate The Gate From Another Element Of An Integrated Circuit," Filed on May 16, 2003; Attorney Docket No.: M-15203 US.					
	AT	United States Patent Application No. 10/440,508, entitled "Fabrication Of Gate Dielectric In Nonvolatile Memories Having Select, Floating And Control Gates," Filed on May 16, 2003; Attorney Docket No.: M-15204 US.					
	AU	United States Patent Application No. 10/440,500, entitled "Integrated Circuits With Openings that Allow Electrical Contact To Conductive Features Having Self-Aligned Edges," Filed on May 16, 2003; Attorney Docket No.: M-15205 US.					
Examiner			Date Considered		6/7/06		
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.							

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		July 30, 2003	Unassigned
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)			
<i>PA</i>	AV	United States Patent Application No. 10/393,212, entitled "Nonvolatile Memories And Methods Of Fabrication," Filed on March 19, 2003; Attorney Docket No.: M-12902 US.	
	AW	United States Patent Application No. 10/411,813, entitled "Nonvolatile Memories With A Floating Gate Having An Upward Protrusion," Filed on April 10, 2003; Attorney Docket No.: M-12903 US.	
	AX	United States Patent Application No. 10/393,202, entitled "Fabrication of Integrated Circuit Elements In Structures With Protruding Features," Filed on March 19, 2003; Attorney Docket No.: M-15151 US.	
	AY	United States Patent Application No. 10/631,941, entitled "Nonvolatile Memory Cell With Multiple Floating Gates Formed After The Select Gate," Filed on July 30, 2003; Attorney Docket No.: M-15171 US.	
	AZ	United States Patent Application No. 10/632,007, entitled "Arrays Of Nonvolatile Memory Cells Wherin Each Cell Has Two Conductive Floating Gates," Filed on July 30, 2003; Attorney Docket No.: M-15223 US.	
	BA	United States Patent Application No. 10/631,452, entitled "Fabrication Of Dielectric For A Nonvolatile Memory Cell Having Multiple Floating Gates," Filed on July 30, 2003; Attorney Docket No.: M-15229 US.	
	BB	United States Patent Application No. 10/632,154, entitled "Fabrication Of Gate Dielectric In Nonvolatile Memories In Which A Memory Cell Has Mutiple Floating Gates," Filed on July 30, 2003; Attorney Docket No.: M-15230 US.	
	BC	United States Patent Application No. 10/631,552, entitled "Nonvolatile Memories And Methods Of Fabrication," Filed on July 30, 2003; Attorney Docket No.: M-12902-1P US.	
<i>PA</i>	BD	United States Patent Application No. 10/632,186, entitled "Nonvolatile Memory Cell With Multiple Floating Gates Formed After The Select Gate And Having Upward Protrusions," Filed on July 30, 2003; Attorney Docket No.: M-15241 US.	
	BE		
	BF		
	BG		
	BH		
Examiner <i>SWR</i>		Date Considered <i>6/7/06</i>	
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				Filed Herewith		Unassigned	
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*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
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	BE	Kim, K.S. et al. "A Novel Dual String NOR (DuSnor) Memory Cell Technology Scalable to the 256 Mbit and 1 Gbit Flash Memories," 1995 IEEE 11.1.1-11.1.4					
	BF	Bergemont, A. et al. "NOR Virtual Ground (NVG)- A New Scaling Concept for Very High Density FLASH EEPROM and its Implementation in a 0.5 um Process," 1993 IEEE 2.2.1-2.2.4					
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	BJ						
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